AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A circuit comprising:

an echo cancellation circuit in which a comparator has an input coupled to receive a transmission line analog signal level, the comparator having a ~~substantially~~ discrete time variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level; and

a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols,

and wherein the echo cancellation circuit further includes a discrete time echo cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to an offset control input of the comparator.

2. Canceled.

3. (Currently Amended) The circuit of claim ~~2~~ 1 wherein the filter includes a digital finite impulse response filter whose output is coupled to the offset control input of the comparator.

4. (Currently Amended) The circuit of claim ~~2~~ 1 wherein the offset control input is a digital input to receive a binary value.

5. (Original) The circuit of claim 1 further comprising a sample and hold circuit whose output is coupled to provide the transmission line analog signal level to the comparator.

6. (Original) The circuit of claim 1 wherein the comparator has a differential input provided by first and second differential pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair, and first and second variable current generators coupled to control respective tail currents of the first and second differential pairs.

7. (Currently Amended) The circuit of claim ~~2~~ 1 wherein the driver is coupled to transmit on the same transmission line from which the analog signal level is derived.

8. (Currently Amended) A method comprising:

determining a binary value based on a sequence of data symbols that have been transmitted by a near end driver in a communication link, the binary value being one of a plurality of binary values that are designed to increase a voltage margin of a near end receiver in the presence of echo in the communication link; and

applying the binary value to an offset control input of a comparator in the near end receiver, and applying a transmission line analog signal level of the communication link to an input of the comparator, the comparator having a ~~substantially~~ variable offset that is controllable, via the offset control input, to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level.

9. (Original) The method of claim 8 wherein the plurality of binary values are a sequence determined by a discrete time filter in response to receiving the sequence of data symbols.

10. (Original) The method of claim 9 further comprising, before determining the binary value, transmitting a training pattern of data symbols in the communication link and determining a plurality of coefficients of the discrete time filter based on the training pattern and using the comparator to detect the training pattern, wherein the coefficients are designed to enable the filter to vary an offset of the comparator so that a voltage margin of the near end receiver is increased in the presence of echo.

11. (Original) The method of claim 10 wherein the coefficients are designed to enable the filter to further vary the offset of the comparator so that an outbound wave is subtracted from the transmission line signal.

12. (Original) The method of claim 8 further comprising using a sample and hold circuit to obtain the transmission line signal level.

13. (Currently Amended) A system comprising:

a printed wiring board on which a ~~parallel~~ bus is formed, an integrated circuit (IC) chip package being operatively installed on the board to communicate using the ~~parallel~~ bus, the package having an IC chip that includes a logic function section and an I/O section as an interface between the logic function section and the bus, the I/O section having a bus receiver in which an echo cancellation circuit includes a comparator that has an input to receive a ~~parallel~~ bus analog signal level, the comparator having a ~~substantially~~ variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the ~~parallel~~ bus analog signal level and the variable reference level, wherein the comparator has a differential input provided by first and second differential pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair, and first and second variable current generators coupled to control respective tail currents of the first and second differential pairs.

14. (Original) The system of claim 13 wherein the logic function section is a microprocessor.

15. (Original) The system of claim 13 wherein the logic function section is a memory controller.

16. (Original) The system of claim 13 wherein the logic function section is a bus bridge.

17. (Original) The system of claim 13 further comprising a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols

and wherein the echo cancellation circuit further includes a discrete time echo cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to an offset control input of the comparator.

18. (Currently Amended) An article of manufacture comprising:

a machine-readable medium having instructions stored thereon which, when executed by a processor, cause an electronic system to display a representation of an echo cancellation circuit in which a comparator has an input to receive a transmission line analog signal level, the comparator having a ~~substantially~~ variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level, a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols received at its input, and wherein the representation of the echo cancellation circuit includes a discrete time echo cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to a discrete time offset control input of the comparator.

19. Canceled.

20. (Currently Amended) The article of manufacture of claim ~~16~~ 18 wherein the representation of the comparator includes first and second differential transistor pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair, and first and second variable current generators coupled to control respective tail currents of the first and second differential pairs.